DESIGN FOR LOW-POWER USING MULTI-PHASE AND MULTI-FREQUENCY CLOCKING

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Abstract: In this paper we present a frequency multiplier circuit implemented on a 1.2μm CMOS technology using dedicated design methodology, delay oriented design. The circuit converts a square wave signals in both quadrature – in phase, and eight - in phase square wave signal. It also multiplies the frequency by two and four. The output frequency of this converter, for 1.2μm CMOS technology, extends from 20MHz to 80MHz. This converter is dedicated for design frequency synthesizer using double loop architecture implemented in embedded instrumentation.

Keywords: Low power design, Frequency multiplier, DLL

1. Introduction

Current and future trends in VLSI IC's design for new generation of System-on-Chip (SoC) can be summarized as follows:

- The incorporation of large portions of imported block, such as memories, processor cores, Intellectual Properties (IP) blocks;
- The presence of particular architectural issues, such as internal busses, test access logic (boundary scan, scan chains) and test execution logic (BIST);
- The increasing adoption of fault-tolerant structures, now essential even in consumer electronic products as circuit density increases;
- The higher level of abstraction, since in many cases most of the circuit is scribed at the RT-level in Verilog or VHDL languages;
- With continuing decreasing in feature size and the corresponding increasing in VLSI chip density and operating frequency.

Most circuits and system designs are confronted with the problem of delivering high-performance with a limited consumption of electric power. Some typ-

ical applications motivated by emerging battery operated applications that demand intensive computation in portable environments, we meet today in wireless communications, computing, instrumentation, consumer electronics, biomedical technologies, industry, controls, etc.

General trends concerning power consumption, power density and V_{DD} versus power and current trend are given in Fig. 1 a), b) and c) respectively.

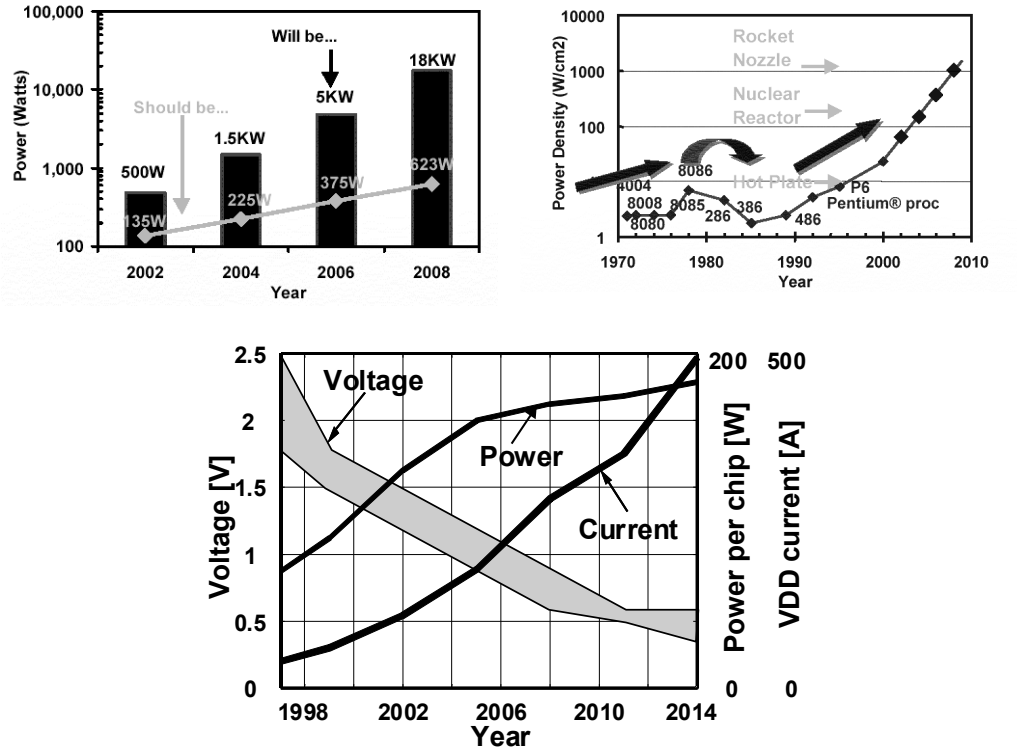

Figure 1: a) Power consumption trend, b) Power density trend and c) V_{DD} versus power and current trend

Bearing in mind the above mentioned (see Fig. 1), efficient methodologies and technologies for the design of high-throughput and low-power digital systems are needed. The main interest of many researches is now oriented towards lowering the power dissipation of these systems while still maintaining the high-throughput in real time processing. In essence, not all part of the VLSI IC may need to function during each clock cycle at maximal speed, i.e. some components may be idle or low active in some clock cycles. Recognizing this fact, during last decade, several low-power design techniques have been proposed, based on the idea of decreasing activity of the some parts within VLSI

IC [1], [2]. The term power manager refers to such techniques in general. Applying power management to a design typically involves two steps [3]: a) identifying idle or low active conditions for various parts of the circuit; and b) redesigning the circuits in order to eliminate or decrease switching activity in idle or low-active

This paper describes a suitable strategy for multi-frequency and multi-phase clock supply or various parts of the VLSI IC based on using delay locked loop (DLL) for controlling activities of different modules without decreasing IC's throughput. The rest of the paper is organized as follows. Section 2 deals with sources of power consumption in VLSI ICs. Section 3 concentrates on power management techniques. Section 4 presents the concept of the multi-phase and multi-frequency generator, and gives some results concerning simulation of tracking jitter and timing error accumulation. Finally our work is summarized in Section 5.

2. Sources of power consumption

The three major sources of power consumption in digital CMOS circuits are [1]:

$$P_{avg} = p_t \cdot C_L \cdot V_{dd}^2 \cdot f_{CLK} + I_{SC} \cdot V_{dd} + I_{leakage} \cdot V_{dd} \qquad (1)$$

The first term represents the capacitive switching power, and is dominant source of power consumption in CMOS gate. Here, C_L is the loading capacitance, f_{clk} is the clock frequency, p_t is the possibility that the power consumption transitions occurs and corresponds to the average number of transitions to clock cycle, and V_{dd} is the supply voltage. The second term is due to the direct-path short circuit current I_{sc}, and arises when a current flows from V_{dd} to ground through both NMOS and PMOS transistors during the rise and fall times of the input and output waveforms. Finally, leakage current $I_{leakage}$, which arises from substrate injection (diode leakage current) and subthreshold effects (subthreshold leakage current) is determined by fabrication technology considerations. The first two terms are dynamic sources of power consumption, i.e. they contribute to power only during transitions, while the third is static one.

Research and design efforts aimed at low power are largely focused on reducing the capacitive switching power as a dominant source of power consumption. The parameters V_{dd}, f_{CLK}, C_L and p_t provide avenues for power reduction. The idea is to either reduce each of the parameters individually without adversely impacting the others or to trade them off against each other [4]. In general: a) Reduction in power through simply a reduction in f_{CLK} is an option acceptable when some components may be idle or low-active during opera-

tion; b) Reduction in V_{dd} is the most effective way for power reduction, since the power is proportional to the square of V_{dd}. However, the problem with reducing V_{dd} is that it leads to an increase in circuit delay. As a solution, the increased delay can be overcome if device dimensions are also scaled down along with V_{dd}, and the main trend now is to integrate as much functionality on a chip as possible; c) The product $p_t \cdot C_L$ is called the average switched capacitance per cycle and the main directions for reducing this capacitance are done at system-, architectural-, RTL-, circuit- or technology level. The design of low-power can be tacked at different level. Starting from system level, passing-through algorithm-, architecture- and circuit-level, and ending with technology level. More details concerning this subject can be found in [4], [5].

3. Power management

We will concentrate now on those techniques that minimize power consumption using clock gating, multiple frequency and poly-phase clocking system. To implement an efficient solution some power management scheme is necessary to involve. The term power-management refers to design methodology that dynamically reconfigures an electronic system to provide the requested services and performance level with a minimum number of active parts or a minimum load on such parts. We define a part as a component or a module within the VLSI IC. In general, a system controller coordinates the activity of the part. For instance, in computer system, global coordination is performed by the operating system [3], [6].

3.1 Power reduction using clock gating

From designer viewpoint a VLSI IC is a set of interacting parts some of which are power-controllable and make up the baseline power consumption that cannot be reduced by power management. Table 1 shows a classification of various frequency controllable low-power approaches.

parameter	non-controllable	controllable	
	active-state	low-active state	idle
f_{CLK}	• single phase • multi-phase	• clock-gating • multiple frequency • frequency scheduling • single (multi)–phase clocking	• clock-gating

Table 1: Frequency controllable low-power method

The parts (modules) of the VLSI IC can be in one of the three states. Some parts can be in active (or dynamic) state performing useful computation at full speed, the other parts can be in low-active state performing useful computation at frequencies less than maximal, or in idle (or standby) waiting for external trigger.

3.2 Power minimization using multiple frequencies

Multiple frequency on the chip, as less aggressive approach is attracting attention. These techniques (see Fig. 2) are standardly used in VLSI ICs in order to reduce the power dissipation while maintaining the operating speed (usually $f_{CLK} \geq f_i$, i=1,..,4). Among the most critical circuit in this approach is the local oscillator realized by a phase-locked loop (PLL) synthesizer, because of poor quality of the voltage-controlled oscillator (VCO) integrated inductance. The multiple frequency method delivers several frequencies of clock signals in accordance with the required performance of each part. The clock frequency is scheduled depending in data load [7]. This has the advantage of allowing parts on the critical paths to use the highest frequency (thus meeting required timing constraints), while allowing parts on noncritical paths to use lower frequencies (reducing the power consumption).

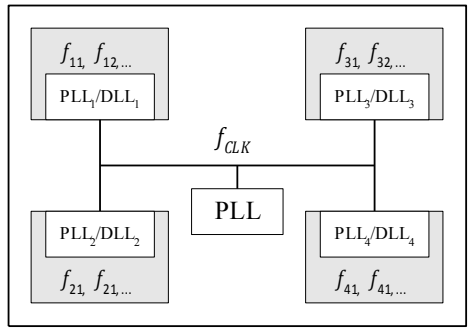

Figure 2: Clock distribution architecture using PLL or DLL

In general, the power spent in a clock network is the largest contributor to the total power in high-performance CPU [5]. One of the standard approaches that are used to reduce power consumption in clock network is clock-gating. Fig. 3 presents the mechanisms of clock gating in the clock distribution network.

Clock-gating reduces the dynamic-power consumption since the clock signal are only distributed to operating parts of the VLSI IC.

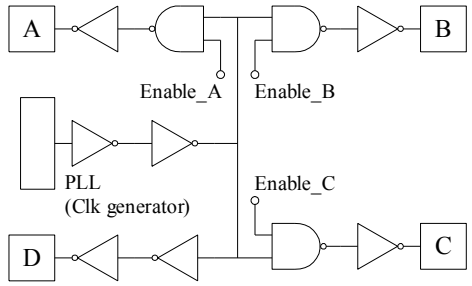

Figure 3: Clock-gating and clock networks

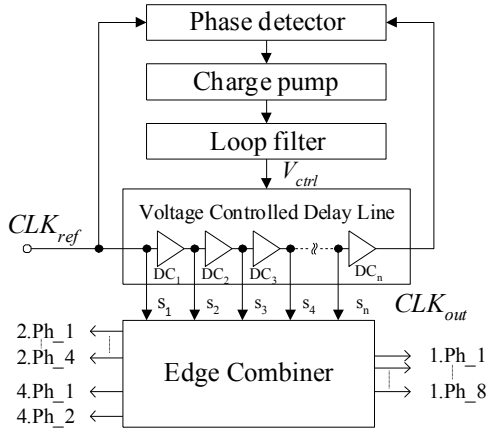

Figure 4: Multi-frequency and multi-phase DLL frequency synthesizer

3.3 Multi-frequency and multi-phase clocking

Recent high-performance VLSI ICs have multiple parts operating with multi-frequency and multi-phase clocks to achieve higher performance. There are two conventional architectures for multi-frequency and multi-phase clock supplies. One is a multi-phases clock distribution architecture, in which a multi-frequency and multi-phase clock is distributed from a phase locked loop (PLL) installed within each part of the VLSI IC [8]. Second conventional architecture employs a single clock distribution also but this architecture uses a DLL to generate multi-frequency and multi-phase clock signal at each part within the VLSI IC [7].

4. Multi-frequency and multi-phases DLL frequency synthesizer

Our proposal uses delay oriented design methodology and is based on a conventional DLL (see Fig. 4). The circuit contains voltage-controlled delay line

(VCDL), a phase detector, charge pump, and first order loop filter. The delay line, consisting of cascaded variable delay stages (cells), is driven by the input reference clock, CLK_{ref}. The output of the delay line's final stage and CLK_{ref} falling (raising) edges are compared by the phase detector to determine the phase alignment error. The phase detector output is integrated by the charge pump and loop filter capacitor to generate the control voltage V_{ctrl} of the delay cells. When correctly locked the total delay line should equal one period T_{ref} of the reference clock CLK_{ref}. The clock reference CLK_{ref} with T_{ref} periodicity propagate trough n delay line cells, providing n asymmetrical square ranges s_i, i=1,..,n with T_{ref} periodicity. These signals differ from clock reference by $\tau_n = n * t_d$ (n=1,..,n) where t_d is the propagation delay of the a single cells (for more details see Fig. 5d).

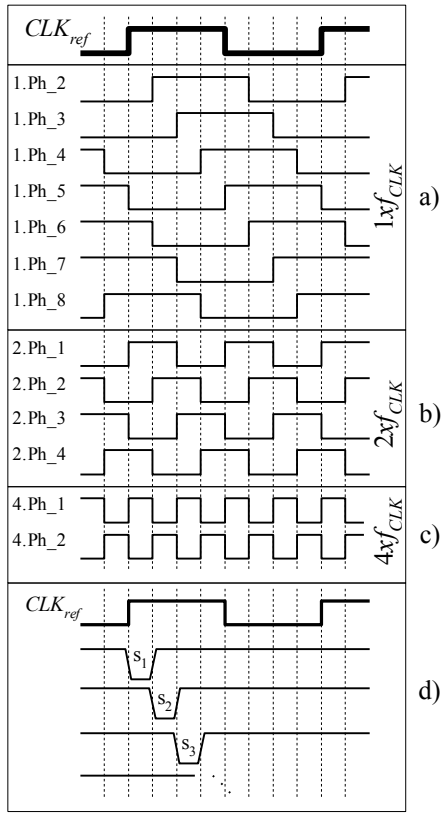

Figure 5: Poly-phase and referent clock multiplier

The constituent Edge-Combiner (Fig. 4) acts as a multi-phase and referent clock multiplier. At its outputs it generates m multiphase-clock signals denoted as 1.Ph_1 to 1.Ph_m (see Fig. 5a, for m=8). In addition it can generate signals with higher frequency than the clock reference (see Fig. 5b and 4c for multi-

phase signals 2.Ph_1 to 2.Ph_4 and 4.Ph_1 to 4.Ph_2 that correspond to 2*f_{CLK} nd 4*f_{CLK}, respectively).

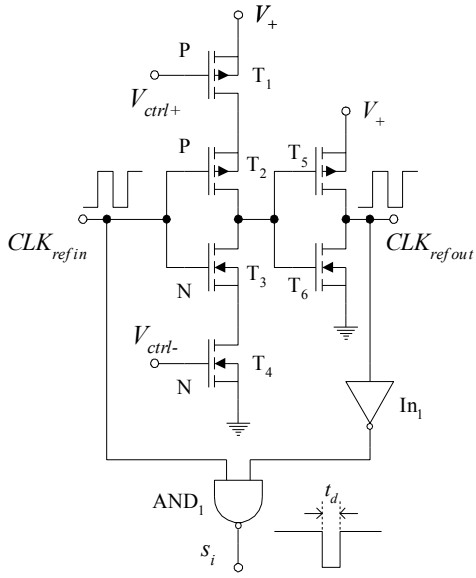

Figure 6: Voltage controlled delay cell with pulse generator

Figure 6 shows one of the VCDL delay cell. The delay cell consists of six transistors and has a non-inverter type structure which guarantees output pulses with sharp rising and trailing edges. Two MOS transistors T_1 and T4 control the propagation delay. T_2 and T_3 form the input inverter, while T_5 and T_6 the output inverter of the delay cell. Combining input and output pulses of the delay cell by the inverter In_1 and gate AND_1 an asymmetrical square wave signal s_i (i=1,..,8) is generated (see also Fig. 5d for more details). Figure 7a and 7b illustrate the logic structures of the frequency multiplier. Figure 7a gives the schematic of the four-phases frequency doubler, while Fig. 7b corresponds to two-phases of the frequency multiplier by four.

As it was already mentioned we use delay oriented design approach based on DLL because of lower jitter accumulation from one cycle of the reference clock to another. The jitter performance of the DLL is degraded by various noise sources, typically in the form of supply and substrate noise in highly integrated circuits. To reduce the jitter, the loop bandwidth should be set as high as possible but must have an upper limit for stability issues. Thus, low jitter DLL designs strongly depend on the delay characteristics of the delay line with supply voltage injection.

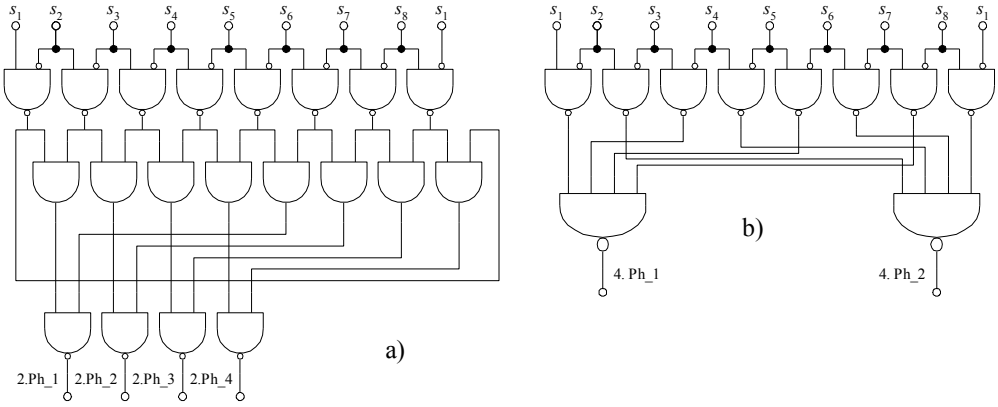

Figure 7: a) Four phases double fCLK frequency multiplier; b) Two phases quadruple fCLK frequency multiplier

It should be noted that simulation results indicate that with the noise generation circuit injecting a ±100mV the peak-to-peak tracking jitter increases to 620ps. Simulation was done with PSpice 9.2 software by using models for 1.2μm CMOS double-metal and double-poly technology.

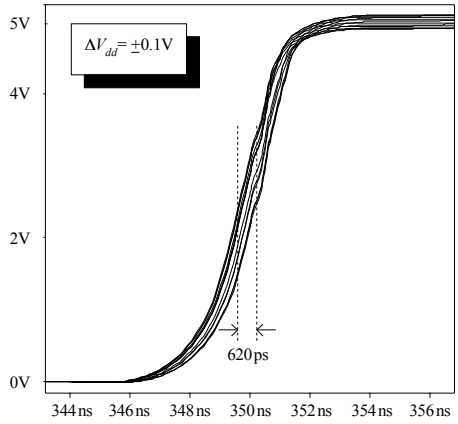

Figure 8: Simulated tracking jitter with ±100mV supply noise

4.1 Jitter influence

A DLL based frequency multiplier (see Fig. 4) using voltage-controlled delay chain has an inherent advantage over a PLL using a voltage-controlled ring oscillator as a standard solution for frequency multiplier. Fig. 9 shows timing jitter accumulation for an oscillator compared with that of a DLL-based frequency multiplier.

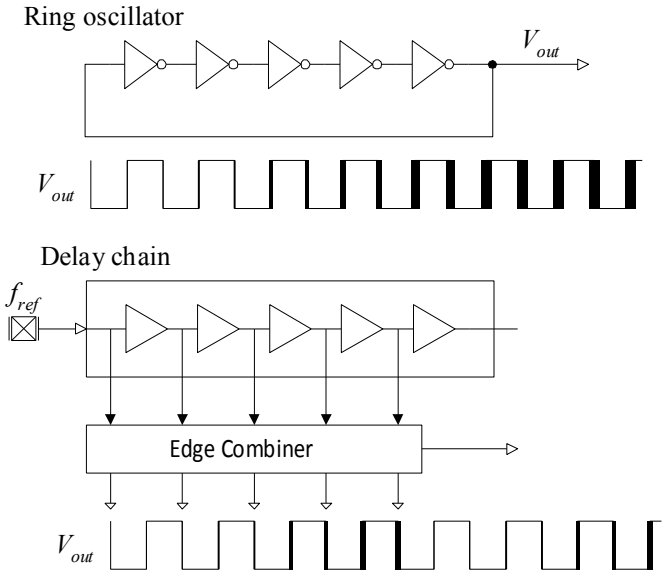

Figure 9: Timing jitter accumulation for ring oscillator vs. delay chain

In the oscillator based solution (Fig. 9a) the random timing error accumulates because the timing jitter at the end of each oscillation is the starting point of the next. In contrast, for finite-length delay chain in the DLL-based frequency multiplier, random timing error accumulates only within a single delay chain cycle [9]. Timing error accumulation for eight-stage delay chain is shows in Fig. 10.

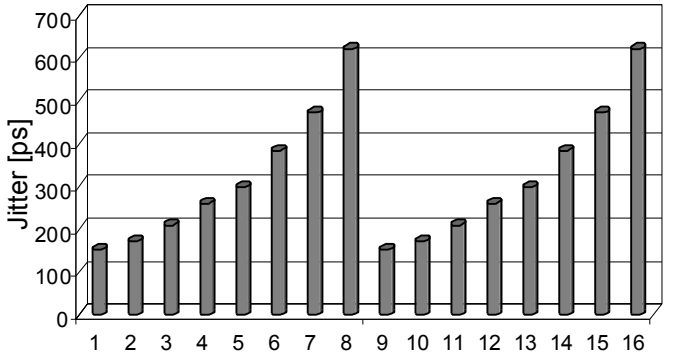

Figure 10: Timing error accumulation for eight-stage delay chain at 20MHz

5. Conclusion

An accurate yet simple multi-frequency and multi-phase clock generator based on delay oriented design methodology is described in this paper. The generator is intended for multi-phase and multi-frequency clock distribution of 1.2μm CMOS low power VLSI IC that have implemented power manager, for frequency and phase switching. It can operate from 20 to 80MHz, with range of phase error within $\pm 2.3^{o}$. This converter is dedicated for design frequency synthesizer using double loop architecture implemented in embedded instrumentation.

6. References

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